

FIG. 1 (Prior Art)

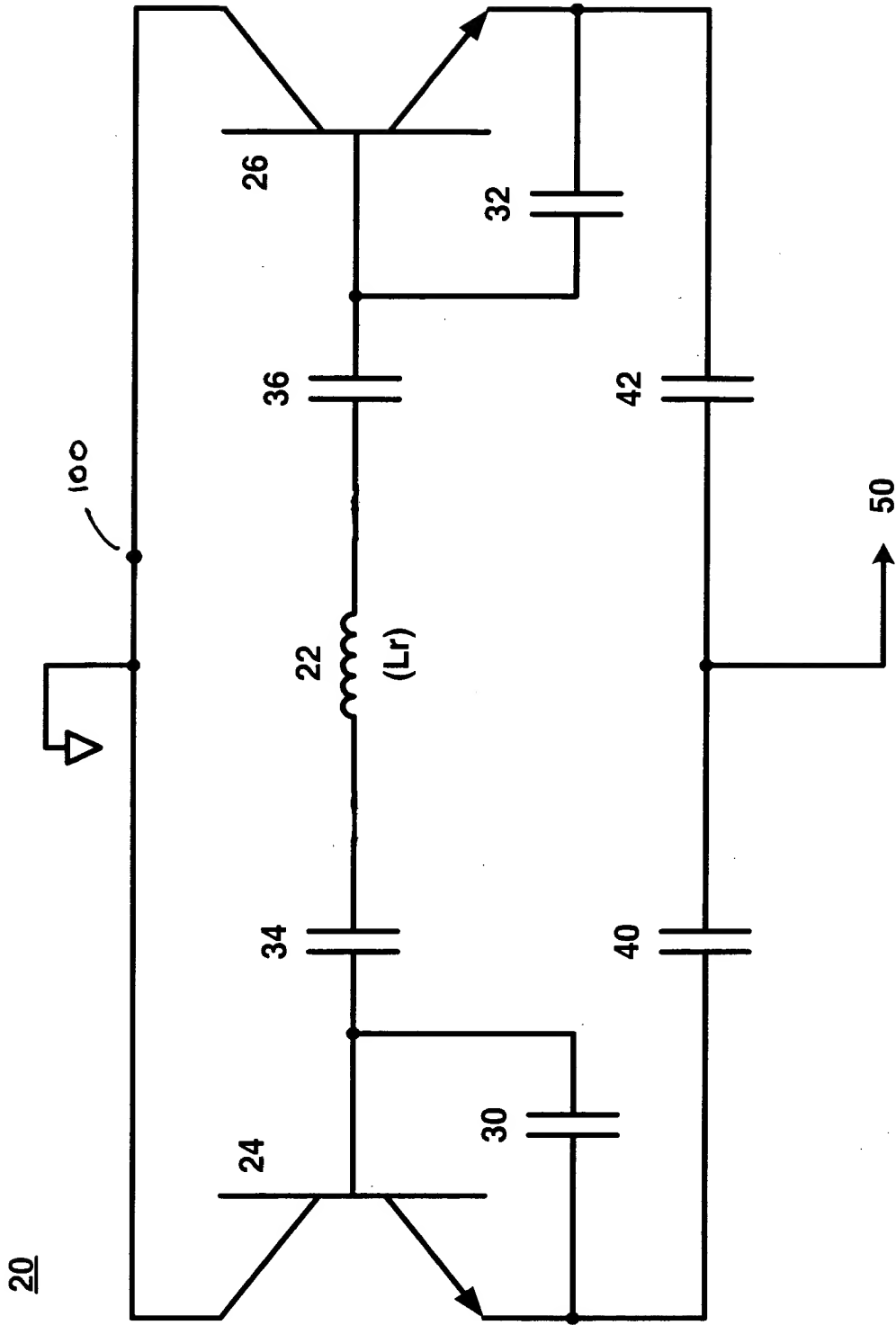


FIG. 2

100mV 10ns 20ns 30ns 40ns 50ns 60ns 70ns 80ns 90ns 100ns

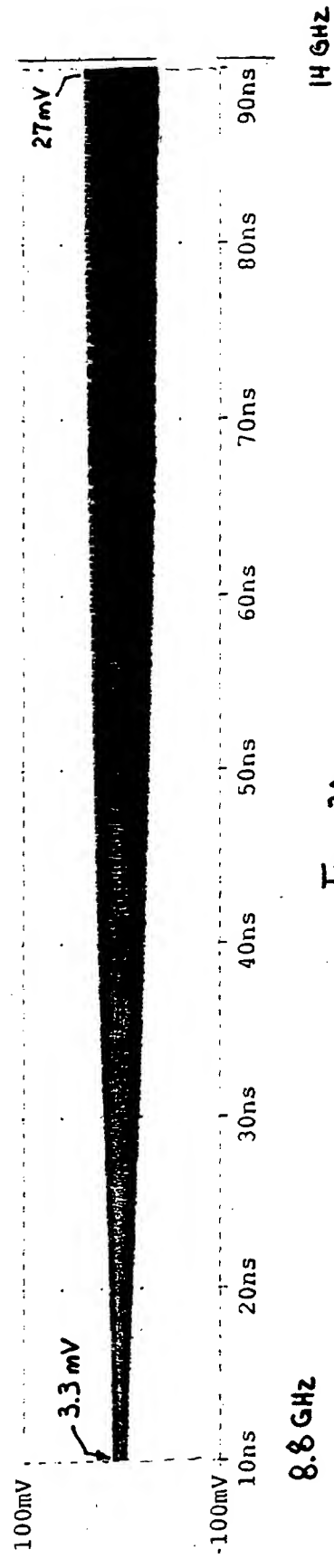


Fig. 3A

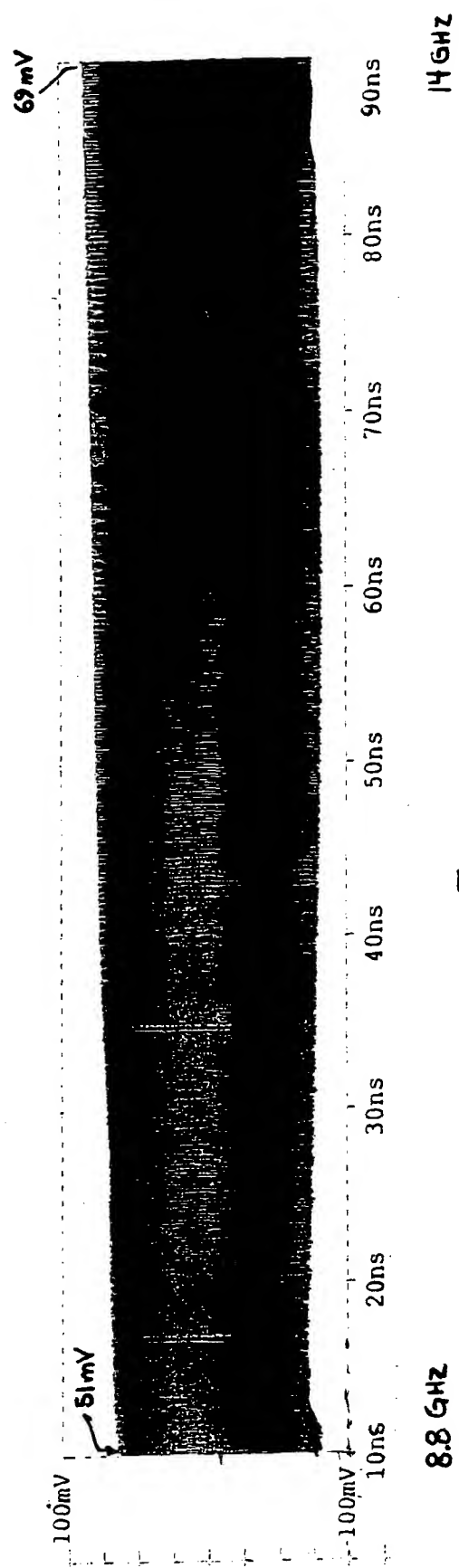


Fig. 3B



FIG. 4

FIG. 6 is a schematic diagram of a circuit 100 in accordance with the present invention. The circuit 100 includes a first input terminal 24, a second input terminal 26, a first output terminal 50, and a second output terminal 52. The circuit 100 also includes a first inductor 22A, a second inductor 22B, a third inductor 22C, a first capacitor 54, a second capacitor 56, a third capacitor 58, a first resistor 60, a second resistor 62, and a third resistor 64. The circuit 100 is configured to provide a first output signal 50 and a second output signal 52 in response to a first input signal 24 and a second input signal 26.

20B

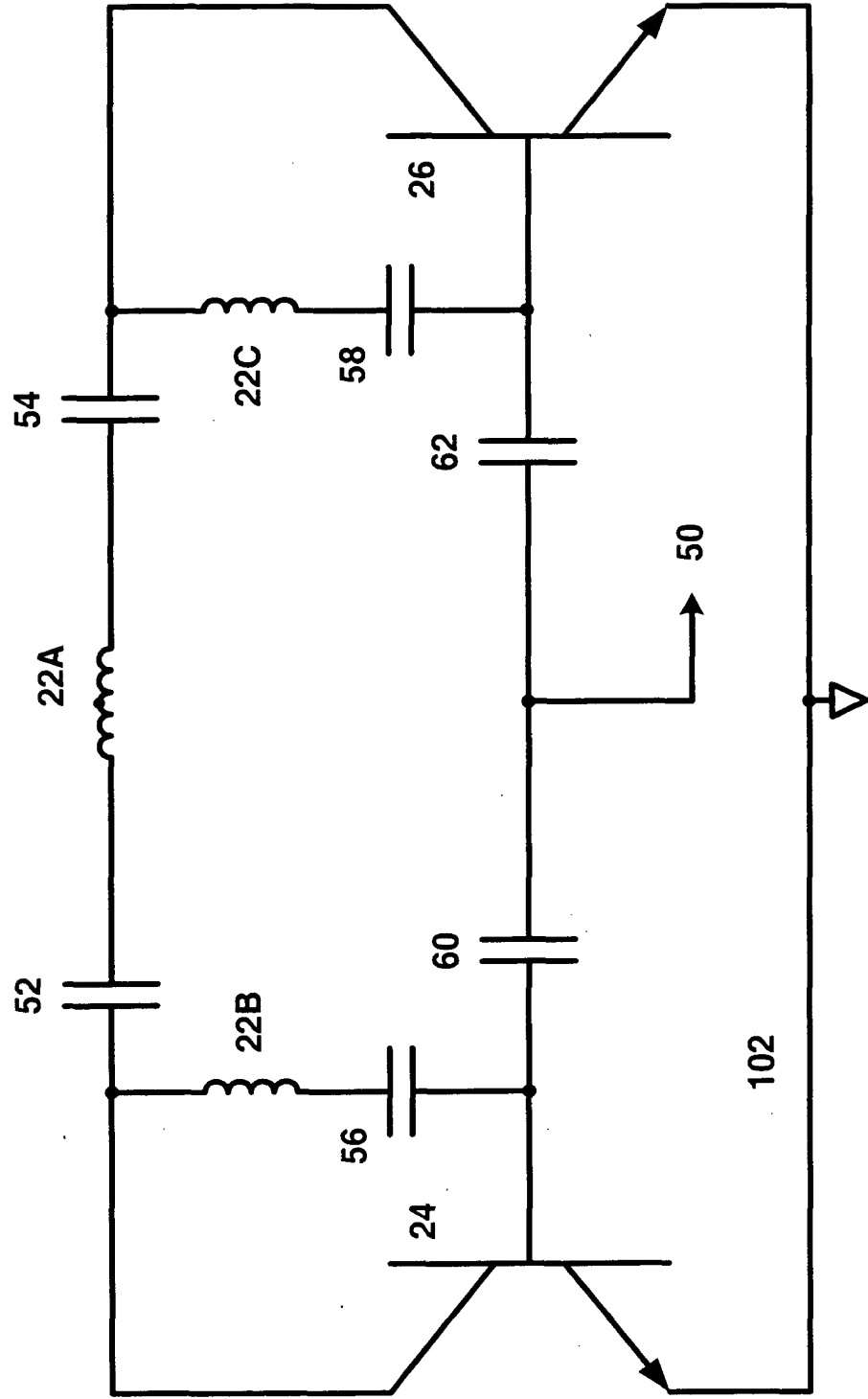


FIG. 6

FIG. 7 is a schematic diagram of a circuit in accordance with the present invention.

20C

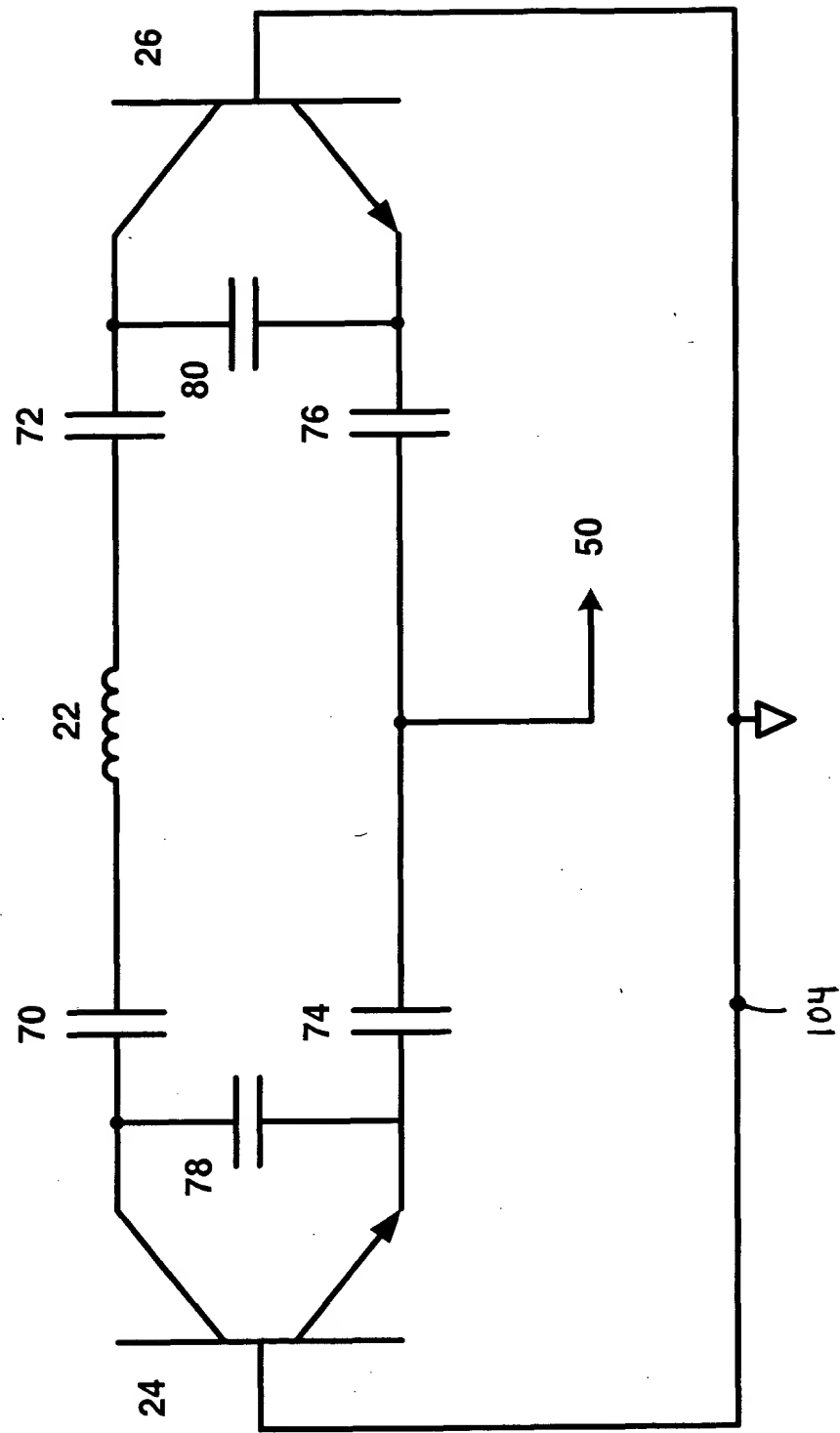


FIG. 7

20D

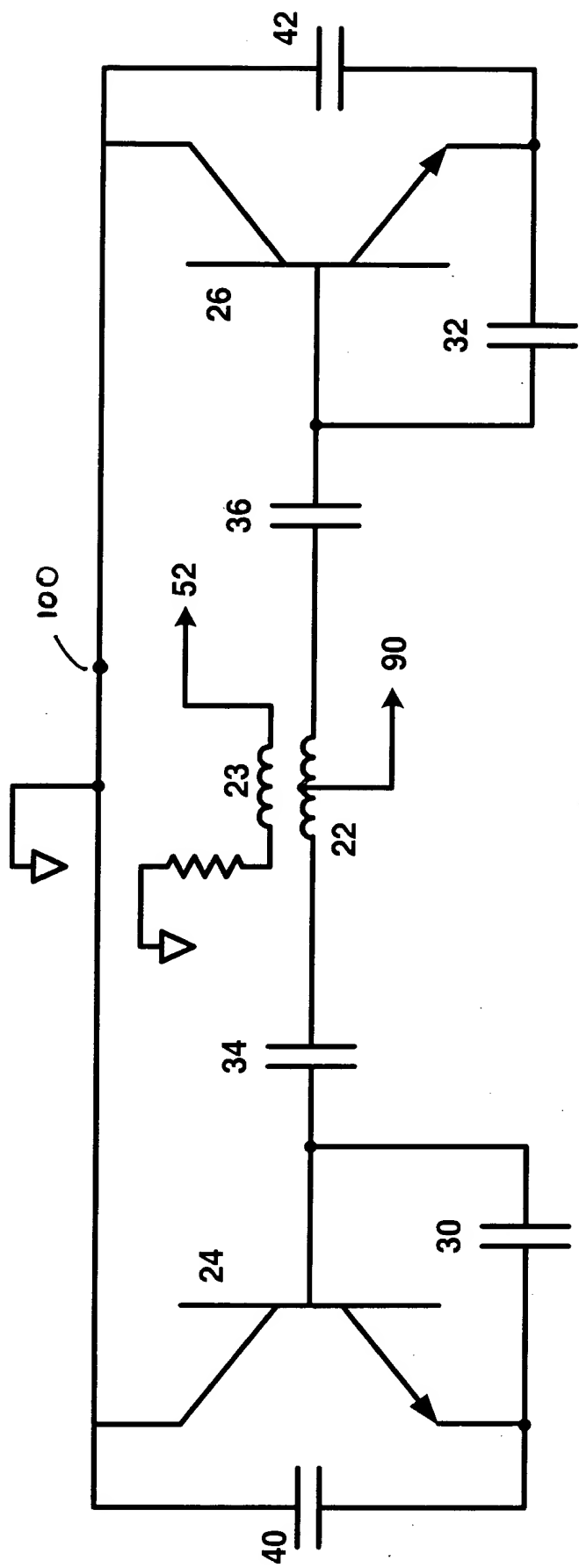


FIG. 8

FIG. 9 is a schematic diagram of a circuit 100, including a transformer 22, a resistor 23, a capacitor 30, a capacitor 32, a capacitor 34, a capacitor 36, a capacitor 40, a capacitor 42, and a diode 50. The circuit 100 is connected to a power source 20E. The transformer 22 is connected to the power source 20E through the capacitor 34. The resistor 23 is connected to the transformer 22 through the capacitor 36. The capacitor 30 is connected to the transformer 22 through the capacitor 32. The capacitor 40 is connected to the transformer 22 through the capacitor 42. The diode 50 is connected to the transformer 22 through the capacitor 34.

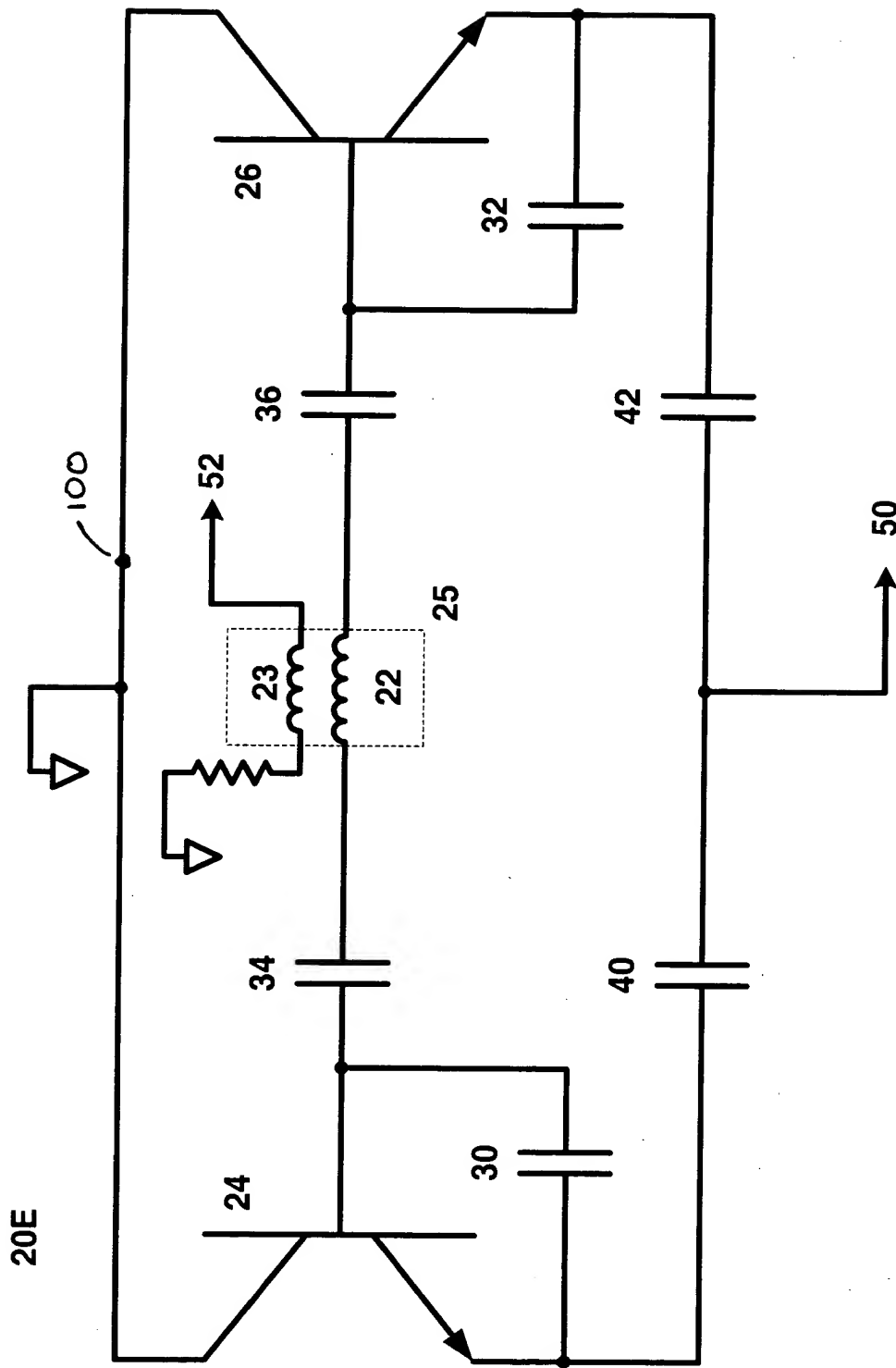


FIG. 9

20E

